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10/037,537	01/02/2002	Delbert Raymond Cecchi	ROC920010213US1	7317

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,537	CECCHI ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-12* is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☒ Claim(s) *2-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/02/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,304,106. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of the instant application has similar scope and all the limitations of claim 1 in the US Patent except:

- claim 1 of the US Patent claims in the preamble "*a Complementary Metal Oxide Semiconductor (CMOS) bi-directional current mode differential link with pre-compensation*";
- claim 1 of the instant application claims in the preamble "*a Complementary Metal Oxide Semiconductor (CMOS) bi-directional current mode differential link*";

- *Prima facie case of obviousness*: In claiming a CMOS bi-directional current mode differential link as set forth in the claimed application, the instant application omits limitations "*with pre-compensation*" in the US patent. Because omission elements in the claim would make the claim broader in the instant application, therefore, it would have been obvious for one of ordinary skill in the art that claim 1 in the instant application is merely an obvious variation of the claims in the US patent. In light of the foregoing discussion, broad claim in the instant application is rejected as obvious double patenting over previously patented narrow claim.

- claim 1 of the US Patent further claims "*a CMOS receiver coupled to both said transmission line and replica driver output; said CMOS receiver subtracting said replica driver output from a signal at said transmission line*".
- claim 1 of the instant application further claims "*a CMOS receiver coupled to both said transmission line and replica driver output; said CMOS receiver comprising a resistor summing network and a differential amplifier*".
- *Prima facie case of obviousness*: The US Patent does not expressly disclose the CMOS receiver comprising a resistor summing network and a differential amplifier as claimed in the instant application. Nevertheless, as claimed in the US Patent claim, the CMOS receiver subtracts said replica driver output from a signal at said transmission line. The act of performing the subtraction is equivalent to the act of summing. In light of the claimed limitations, it would

have been obvious for one of ordinary skill in the art at the time the invention was made that the CMOS receiver includes a summing network for performing subtraction the replica driver output from a signal at the transmission line. Furthermore, referring to figure 2 of the US Patent, two pairs of series resistors connected to the input of receiver 106. Therefore, the summing network includes resistors. And since the receiver 106 receives as differential inputs of replica driver output and a signal at the transmission line, the receiver 106 inherently includes a differential amplifier.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. U.S. Patent 6,507,225 B2 in view of Bosnyak et al. U.S. Patent 5,898,297.

Regarding claim 1, Martin et al. invention is directed to a method and apparatus for providing a simultaneous bi-directional data port circuit that includes a current mode output driver for driving an output node and a current mode return driver for driving a differential receiver; see column 2, lines 15-28. Figure 1 illustrates an electronic system having two integrated circuits with simultaneous bi-directional port circuits.

In column 2, lines 47-65, integrated circuit 110 includes a current mode output driver 124 for receiving data input and having an output coupled to a transmission line, conductors 102 104;

current mode return driver 126 for receiving data output and driving a differential receiver 140. Martin et al. does not teach current mode return driver 126 providing an output substantially equal to current mode output driver 124. Nevertheless, in column 3, lines 6-20, Martin et al. further teaches differential receiver 140 having two sets of differential input nodes, one coupled to differential data lines 144, and the other coupled to differential data lines 148. Because differential receiver 140 subtracts the differential voltage on differential data lines 148 from a differential voltage on differential data lines 144 to produce inbound data on node 142, it would have been obvious for one of ordinary skill in the art at the time the invention was made that current mode return driver 126 provides output substantially equal to current mode output driver 124, and as a result of that, current mode return driver 126 is a replica driver because current mode return driver 126 receives the same data input as current mode output driver 124. The reason for producing substantially equal to current mode output driver 124 is that current mode return driver 126 is needed to drive differential receiver 140.

As recited above, differential receiver 140 having two sets of differential input nodes, one coupled to differential data lines 144, and the other coupled to differential data lines 148. Martin et al. does not expressly disclose differential

receiver 140 comprising a resistor summing network and a differential amplifier as claimed in the instant application. Nevertheless, as claimed in column 3, lines 5-20, differential receiver 140 subtracts the differential voltage on differential data lines 148 from a differential voltage on differential data lines 144 to produce inbound data on node 142. The act of performing the subtraction is equivalent to the act of summing. In light of the foregoing discussion, it would have been obvious for one of ordinary skill in the art at the time the invention was made that differential receiver 140 includes a summing network for performing subtraction the differential voltage on differential data lines 148 from a differential voltage on differential data lines 144 to produce inbound data on node 142. Furthermore, in column 3 line 62 via column 4 line 8, integrated circuit 110 includes resistors 128 130 in combination with current mode output driver 124 and current mode return driver 126 to provide voltage scaling at the input of differential receiver 140. As result of that, resistors 128 130 in combination with summing inputs of differential receiver 140 forms a resistor summing network as claimed. Differential receiver 140 inherently includes differential amplifier.

Referring to figure 3, current mode output driver 124 and current mode return driver 126 includes parallel current sources, wherein each current source is arranged to send positive and negative current through a load responsive to an applied control signal as claimed.

Martin et al. does not teach current mode output driver 124, current mode return driver 126 and differential receiver 140 are implemented with CMOS

technology as claimed. Bosnyak et al. discusses in another US patent that differential drivers are implemented with bipolar and CMOS technology; see column 1, lines 25-35. Bosnyak et al. invention is directed to high speed differential drivers for providing bi-directional output current in response to differential input signals; see column 1, lines 5-10. Bosnyak et al. CMOS differential driver operates at high speed while reducing power dissipation. Martin et al. and Bosnyak et al. teach in the same field of endeavor. Because Martin et al. expresses that integrated circuit 110 can be any type of integrated circuit capable of including simultaneous bi-directional port circuits, it would have obvious for one of ordinary skill in the art at the time the invention was made that Martin et al. current mode output driver 124, current mode return driver 126 and differential receiver 140 can be implemented with CMOS technology as taught in Bosnyak et al. invention. The motivation is that Bosnyak et al. teaches that high speed CMOS differential drivers are well suited in an integrated circuit chip which is similar to Martin et al. integrated circuit 110.

Allowable Subject Matter

3. Claims 2-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 8-12 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 8, claim is allowed over prior art of record since the cited references taken individually or in combination fails to particularly disclose a method as set forth in the application claim. The closest prior art of record, Martin et al. (US 6,507,225 B2) disclosing current mode driver with variable equalization, does teach or suggest the method as claimed in the pending application.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cao et al. U.S. Patent 5,541,535 discloses "CMOS Simultaneous Transmission Bi-directional Driver/Receiver".

Chung et al. U.S. Patent 6,836,290 B1 discloses "Combined Single-Ended And Differential Signaling Interface".

Neal et al. U.S. Patent 6,070,211 B1 discloses "Driver/Receiver Circuitry For Enhanced PCI Bus With Differential Signaling".

Cao et al. U.S. Patent 6,771,675 discloses "Method For Facilitating Simultaneous Multi-directional Transmission Of Multiple Signals Between Multiple Circuits Using A Single Transmission Line".

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

TESFALDET BOCURE
PRIMARY EXAMINER